2 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

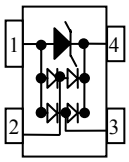
Description

Dual-rail clamp diodes are designed to provide ESD protection for high speed data interfaces. They are ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading.

The UMDSR05 consists of two pairs of diodes in series which steer the positive or negative ESD current pulse to either the positive (Vp) or negative (Vn) supply rail, and a TVS diode which is embedded between Vp and Vn. The ultra low capacitance array configuration allows the user to protect two high-speed data or transmission lines. The TVS diode prevents over-voltage on the power line, protecting any down stream components.

Ultra Low Capacitance Series TVS

SOT-143 Pin Configuration



Pin	Description
1	V/n (GND)
2	I/O
3	I/O
4	Vp

Features

* Solid-state silicon avalanche technology
* SOT-143 package
* Bi-Directional protection
* Protects up to two data lines and one power line
* Ultra Low channel input capacitance of 0.8pF
* Working voltage: 5V
* Low clamping factor Vcl/Vbr
* Low leakage current
* Full RoHS compliance
* Complies with the following standards:
  - IEC 61000-4-2 (ESD) Air-15kv, Contact-8kv
  - IEC 61000-4-4 (EFT) (5/50ns)
  - IEC 61000-4-5 (Surge) (8/20μs)

Mechanical Characteristics

* Molded SOT-143 package
* Weight 9 milligrams (Approximate)
* Available in Lead-Free Pure-Tin Plating
* Solder Reflow Temp: Pure-Tin (Sn), 260-270ºC
* Consult Factory for Leaded Device Availability
* Flammability Rating UL 94V-0
* 8mm Tape and Reel per EIA Standard 481
* Device Marking: Marking Code,

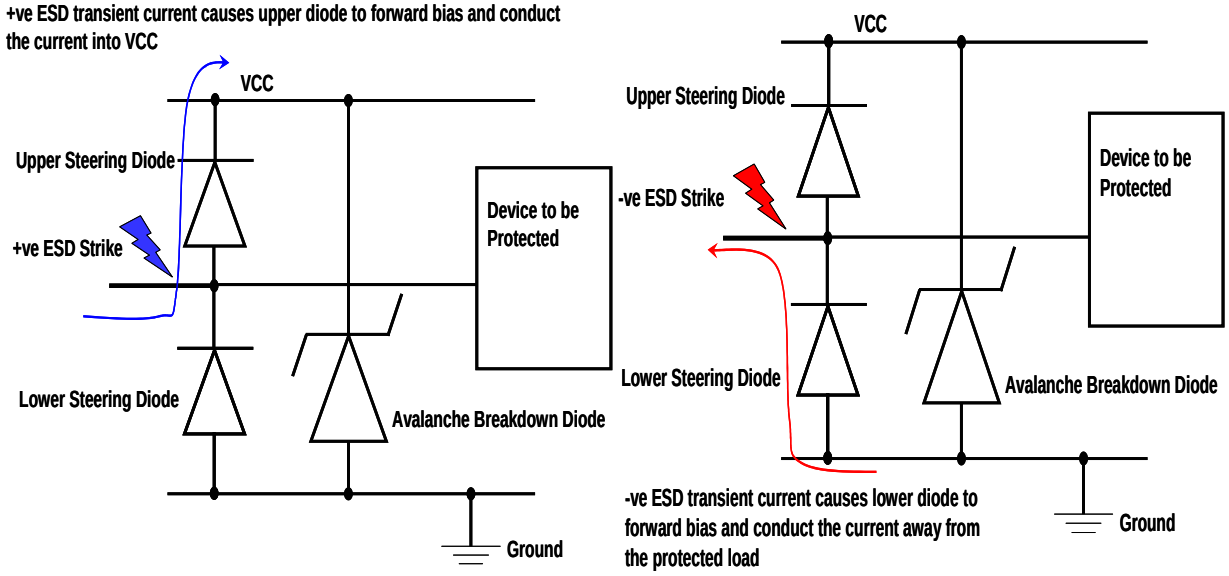
Applications

* USB2.0 Power and Data Line Protection
* Fax machine with USB2.0 Port
* Portable Electronics with USB2.0 Port
* Video Line Protection
* WAN/LAN Equipment Protection
* T1/E1 secondary IC Side Protection
* ISDN S/T Interface Protection

2 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

Absolute Maximum Ratings @ 25ºC unless otherwise specified			
Parameter	**Symbol**	**Value**	**Units**
Peak Pulse Power; pulse waveform = 8/20µs	Ppp	200	W
Peak Pulse Current; pulse waveform = 8/20µs	Ipp	5.4	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	Vpp	±15 ±8	kV
Operating Temperature	Tj	-40 to 125	ºC
Storage Temperature	Tstg	-55 to 150	ºC

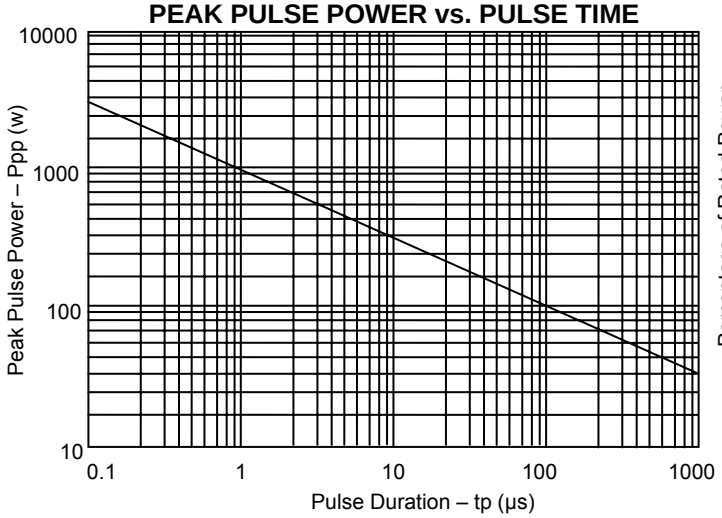
Dual-Rail Clamp Diode Protection



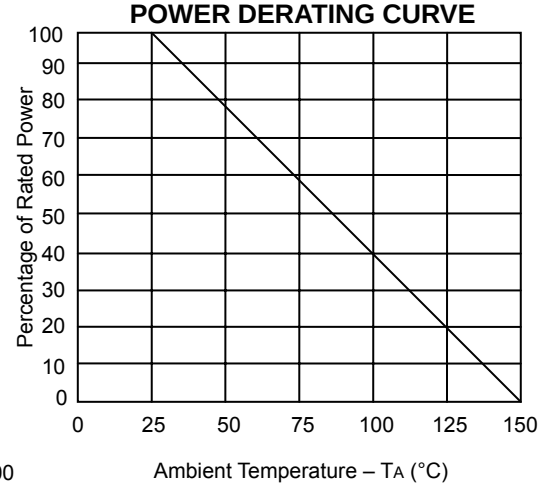
Electrical Characteristics @ 25ºC unless otherwise specified					
Parameter	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
Operating Supply Voltage (Vp)				5.5	V
Operating Supply Current (Ip)	Vp=3.3v			8	µA
Forward Voltage Top Diode Forward Voltage Bottom Diode	If=8mA	0.6 -0.6	0.8 -0.8	0.95 -0.95	V V
Leakage Current	Vp=5v		±0.1	±1	µA
Signal Clamp Voltage	Ipp=10mA	6.5	7.5	9.0	V
Clamping Voltage +ve Transient Clamping Voltage -ve Transient	Ipp=1A, Tp=8/20µs		9 -1.5		V V
Input Capacitance @1MHz	Vp=3.3v,Vi/o=1.65v	0.6	0.8	1.0	pF

Electrical Characteristics Graphs

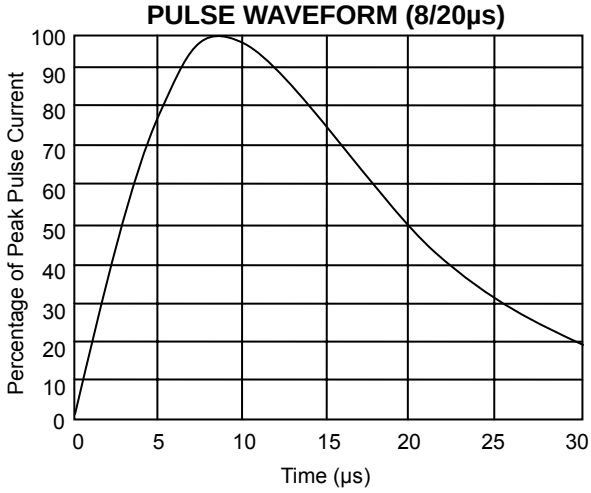
PEAK PULSE POWER vs. PULSE TIME



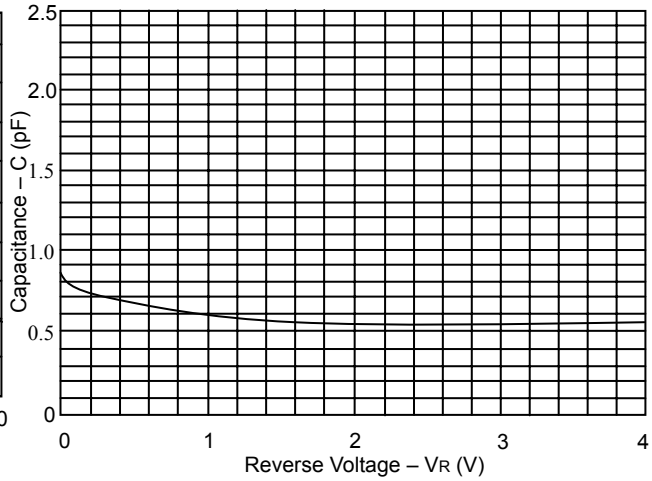
POWER DERATING CURVE



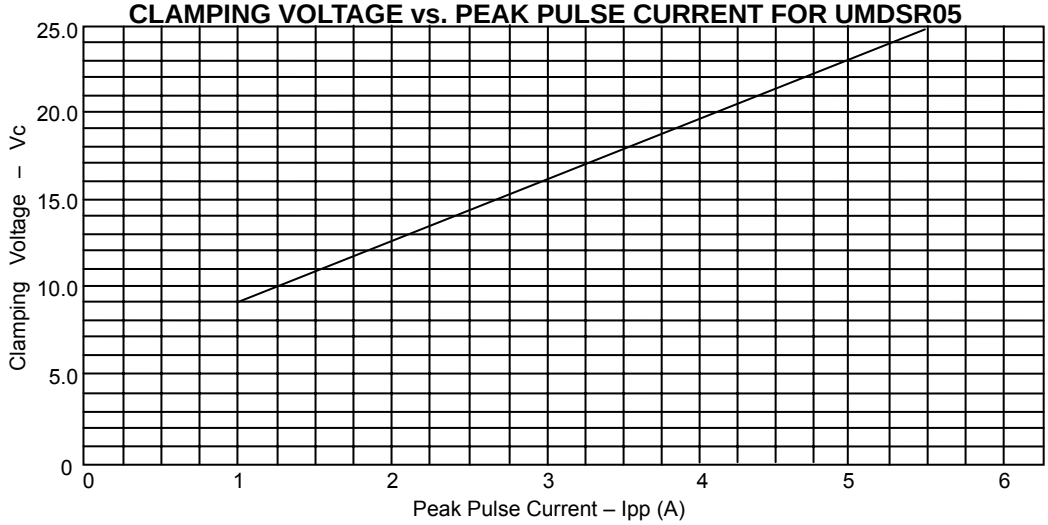
PULSE WAVEFORM (8/20µs)



INPUT CAPACITANCE vs. INPUT VOLTAGE FOR UMDSR05



CLAMPING VOLTAGE vs. PEAK PULSE CURRENT FOR UMDSR05

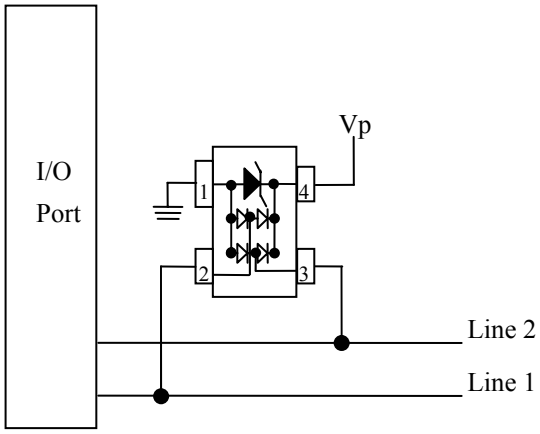


Applications Information

The UMDSR05 has a ultra low typical capacitance of 0.8pF and operates with virtually no insertion loss to 1GHz. This makes the device ideal for protection of high-speed data lines such as USB2.0 and gigabit Ethernet interfaces. The UMDSR05 is designed for use in applications where board space is at a premium. Each device requires less than 7.6mm² of PCB area and will protect up to two data lines and one power line.

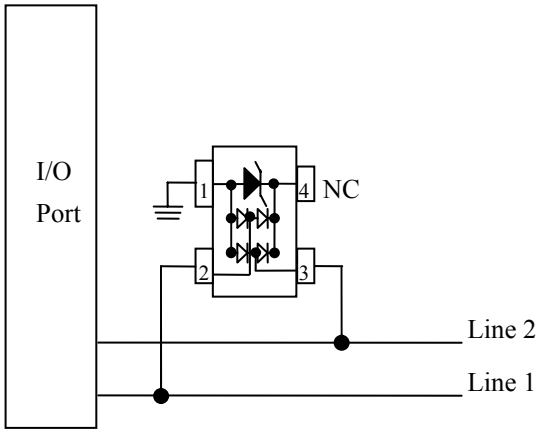
To protect data lines and the power line, connect pin 4 directly to the positive supply rail (Vp). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail.
Circuit connectivity is as follows:

- Line 1 is connected to Pin 2
- Line 2 is connected to Pin 3
- Pin 4 is connected to Vp
- Pin 1 is connected to ground

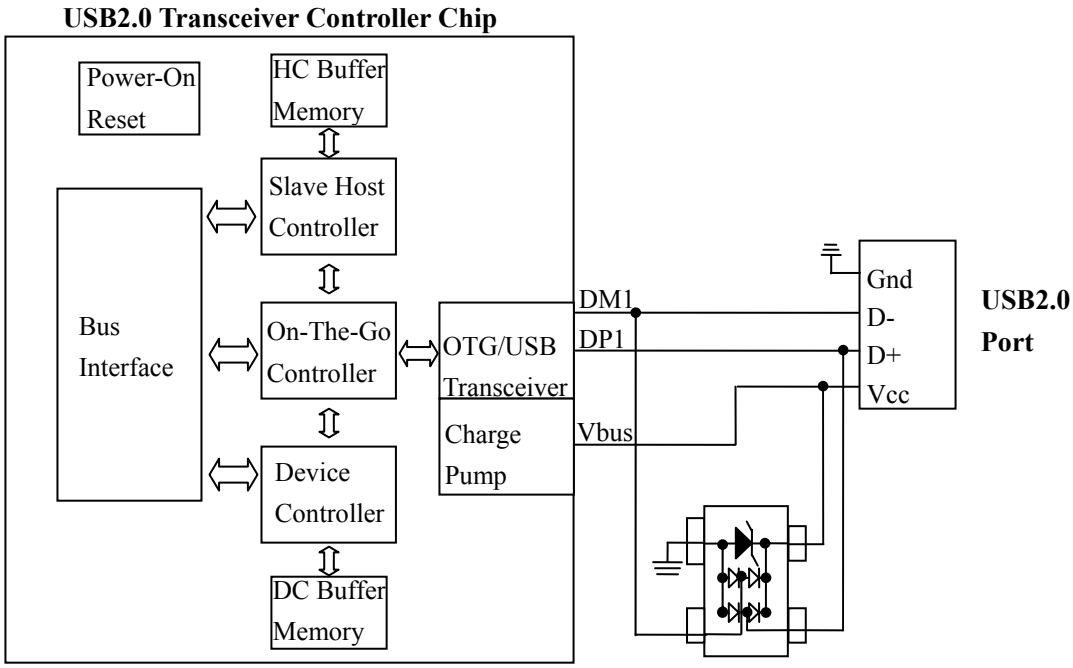


In applications where no positive supply reference is available, or complete supply isolation is desired, the internal TVS may be used as the reference. In this case, pin 4 is not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).
Circuit connectivity is as follows:

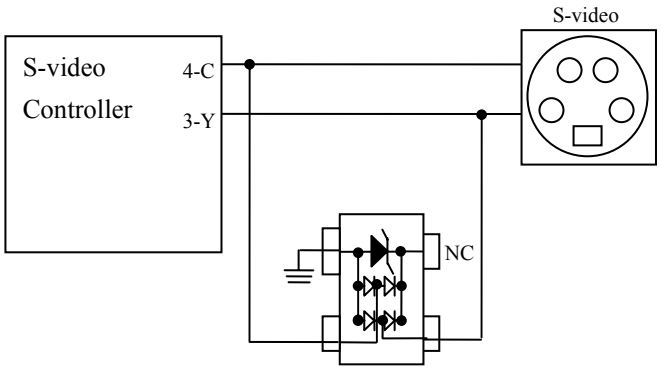
- Line 1 is connected to Pin 2
- Line 2 is connected to Pin 3
- Pin 4 is not connected
- Pin 1 is connected to ground



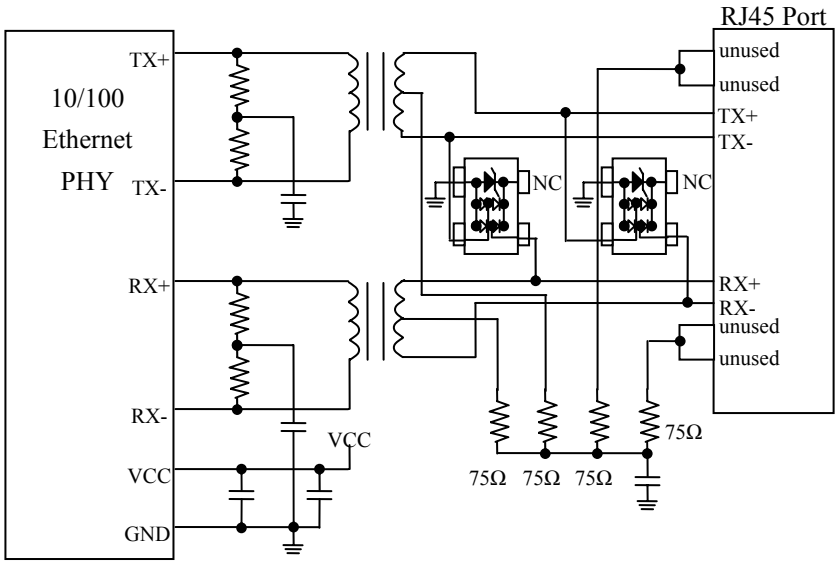
UMDSR05 on USB2.0 Port Application



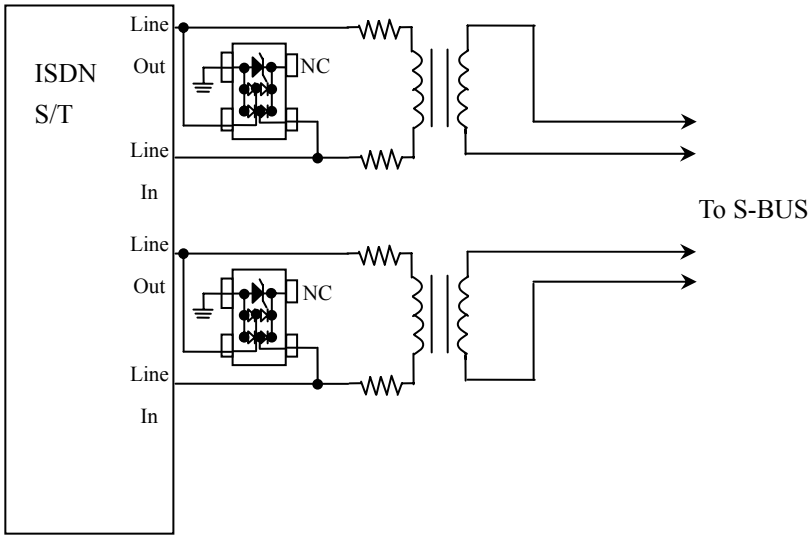
UMDSR05 on S-video Connector Application



UMDSR05 on 10/100 Ethernet Port Application



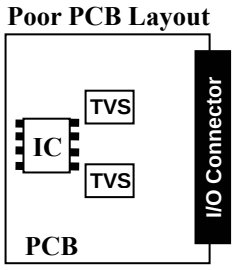
UMDSR05 on ISDN S/T Interface Application

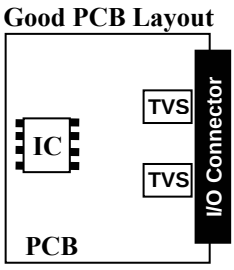


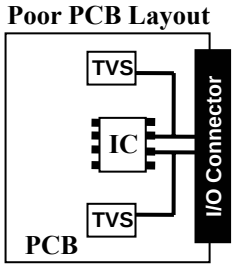
Circuit Board Layout Recommendations

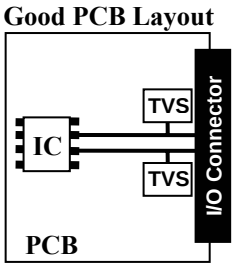
Good circuit board layout is critical for creating an effective surge suppression circuit. The following PCB guidelines are recommended to enhance the performance of a TVS device:

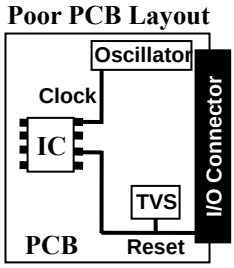
- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- The ESD transient return path to ground should be kept as short as possible.
- Place a TVS and decoupling capacitor between power and ground of components that may be vulnerable to electrostatic discharges to the ground plane.
- Minimize all conductive loops including power and ground loops.
- Use multilayer boards when possible.
- Minimize interconnecting line lengths.
- Never run critical signals near board edges.
- Fill unused portions of the PCB with ground plane.

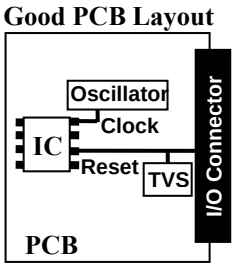










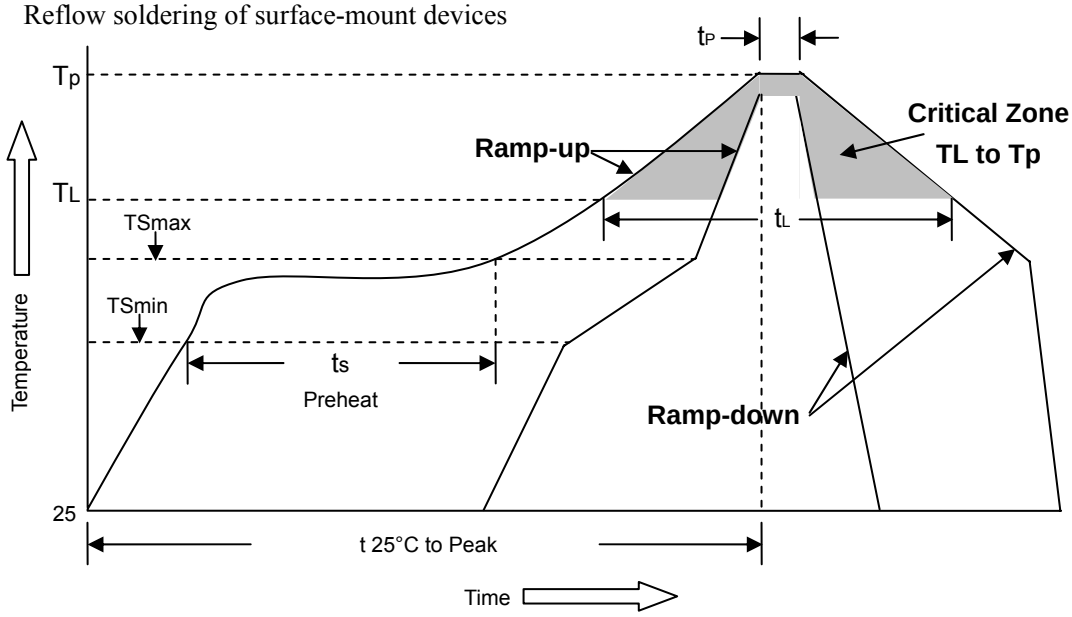


Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. Unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation to solder joint.

Soldering Method for UMD's Products

1. Storage environment: Temperature = 10ºC~35ºC Humidity = 65%±15%
2. Reflow soldering of surface-mount devices



Profile Feature	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	<3ºC/sec
Preheat - Temperature Min (T_{Smin}) - Temperature Max (T_{Smax}) - Time (min to max) (t_s)	 150ºC 200ºC 60~180sec
T_{Smax} to T_L - Ramp-up Rate	 <3ºC/sec
Time maintained above: - Temperature (T_L) - Time (t_L)	 220ºC 50~145sec
Peak Temperature (T_P)	260ºC +0/-5ºC
Time within 5ºC of actual Peak Temperature (t_P)	20~40sec
Ramp-down Rate	<6ºC/sec
Time 25ºC to peak Temperature	<8 minutes

Flow (wave) soldering (solder dipping)

Products	Dipping time
Pb devices	5sec±1sec
Pb-Free devices	5sec±1sec

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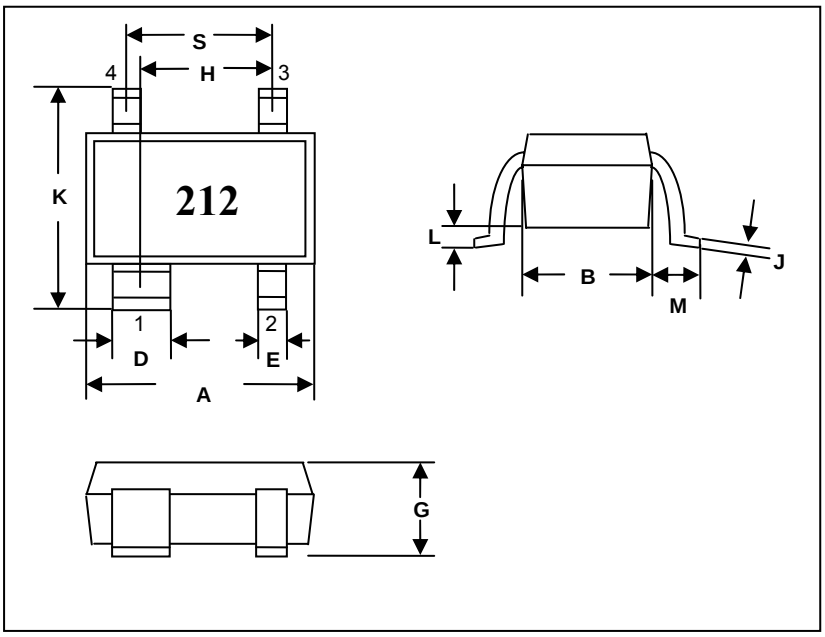
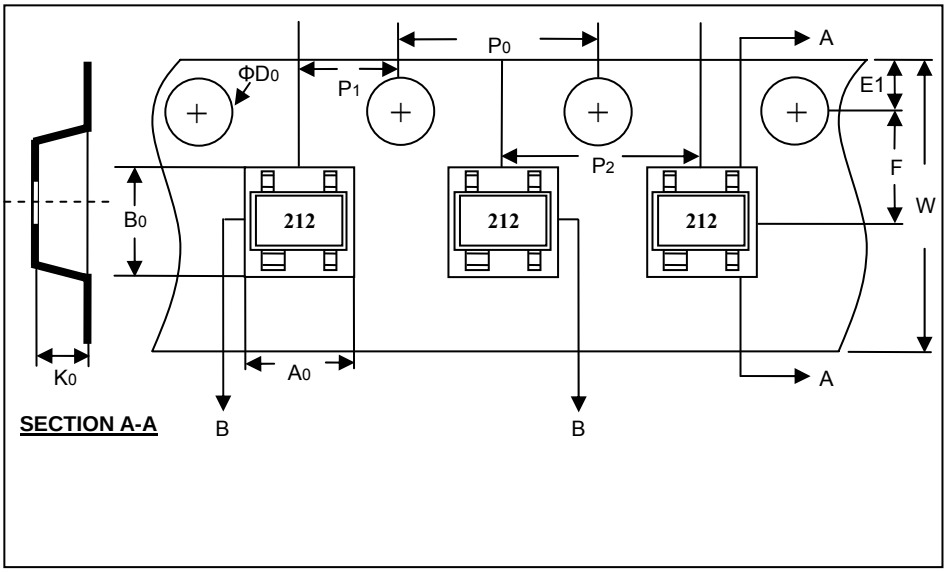
SOT-143 Dimension Drawing

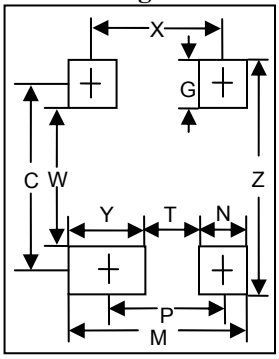


Dimensions				
Dim	Inches		mm	
	Min	Max	Min	Max
A	0.110	0.120	2.80	3.04
B	0.047	0.055	1.20	1.39
D	0.031	0.037	0.79	0.93
E	0.015	0.020	0.39	0.50
G	0.033	0.045	0.84	1.14
J	0.003	0.006	0.08	0.15
K	0.083	0.098	2.11	2.48
L	0.0005	0.004	0.013	0.10
M	0.018	0.024	0.46	0.60
S	0.070	0.080	1.78	2.03
H	0.068 BSC		1.72 BSC	

SOT-143 Carrier Dimension



Mounting Pattern



Typical		
Dim	MM	Inches
Z	2.75	0.108
C	1.90	0.075
W	1.05	0.041
G	0.85	0.033
M	2.85	0.112
X	2.00	0.079
P	1.80	0.071
Y	1.20	0.047
T	0.80	0.031
N	0.85	0.033

Dimensions in mm.

Reel Dia.	Tape Width	A0	B0	K0	ΦD0	E1
178mm (7”)	8mm	3.20±0.10	2.70±0.10	1.35±0.10	1.50±0.10	1.75±0.10
F	W	P0	P1	P2	T	
3.50±0.05	8.00±0.30	4.00±0.10	2.00±0.05	4.00±0.10	0.25±0.02	

Marking Code

Part Number	Device Marking
UMDSR05	212

Ordering Information

Part Number	Lead Finish	Qty Per Reel	Reel Size
UMDSR05	Pb-Free	3,000	7 inch

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