

**DFN-8 Hqwt Lines EMI Filter Array with TVS Diodes**

**Description**

With demand surging for advanced multimedia capabilities in wireless handsets, designers are facing new challenges. In clamshell and slider phone configurations, the interface signals are typically routed on a flexible printed circuit board that is susceptible to EMI. In addition, as sensor resolution increases, these interfaces operate at higher data rates, and maintaining signal integrity becomes a key requirement.

The UMD4D-100L is an EMI filter array which integrate four Pi-filters (C-R-C) with component values of 10pF-100Ohm-10pF. This device includes ESD protection TVS diodes on every pin, which provide a very high level of protection for sensitive electronic components.

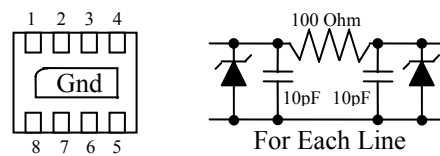
**Features**

- \* Solid-state silicon avalanche technology
- \* DFN-8 package
- \* Bi-Directional EMI filtering
- \* Protects up to four data lines
- \* Better than 30dB of attenuation, 800-3000MHz
- \* Working voltage: 5V
- \* Low pass filter
- \* Low leakage current
- \* Full RoHS compliance
- \* Complies with the following standards:
  - IEC 61000-4-2 (ESD) Air-15kv, Contact-8kv
  - IEC 61000-4-4 (EFT) (5/50ns)
  - IEC 61000-4-5 (Surge) (8/20µs)

**EMI Filter Array TVS**



**DFN-8 Pin Configuration**



<u>Pin</u>	<u>Description</u>
1-4	Input Lines
5-8	Output Lines
Or vice versa	
Center Tab	Ground

**Mechanical Characteristics**

- \* DFN-8 package
- \* Available in Lead-Free Pure-Tin Plating
- \* Solder Reflow Temp: Pure-Tin (Sn), 260-270°C
- \* Consult Factory for Leaded Device Availability
- \* Flammability Rating UL 94V-0
- \* 8mm Tape and Reel per EIA Standard 481
- \* Device Marking: Marking Code,  
Pin one defined by DOT

**Applications**

- \* Cellular Handset CCD Camera Lines
- \* Clamshell Handset Color LCD Protection
- \* Slider Handset Color LCD Protection
- \* Digital Camera
- \* PDA CCD Camera Lines
- \* Microprocessor Based Equipment

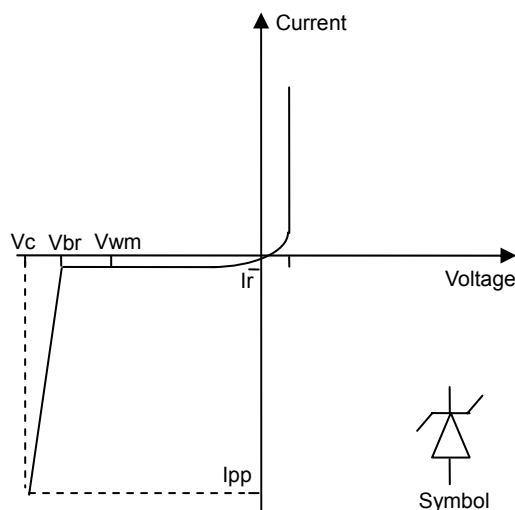
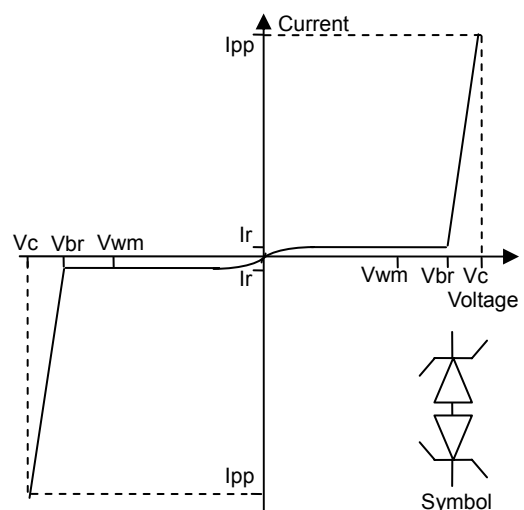
**DFN-8 Hqwt Lines EMI Filter Array with TVS Diodes**
**Absolute Maximum Ratings @ 25°C unless otherwise specified**

Parameter	Symbol	Value	Units
DC Power per Resistor	P	100	mW
Operating Temperature	Tj	-40 to 85	°C
Storage Temperature	Tstg	-55 to 150	°C

**Electrical Characteristics @ 25°C unless otherwise specified**

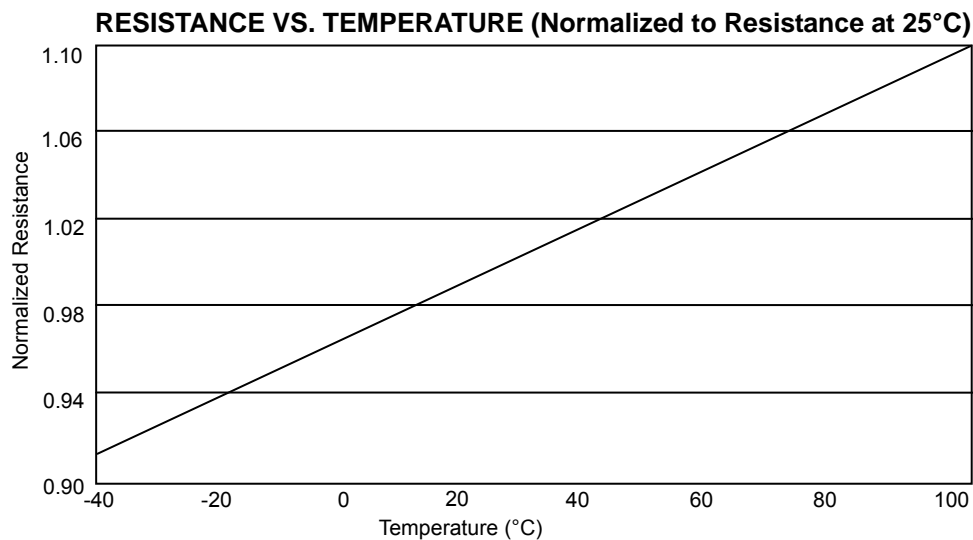
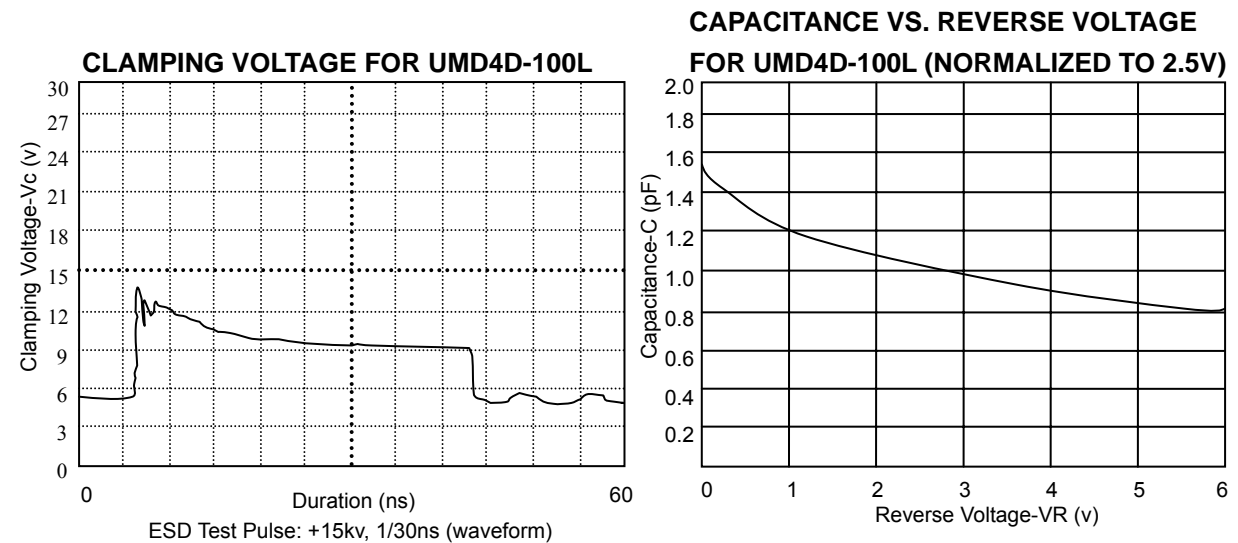
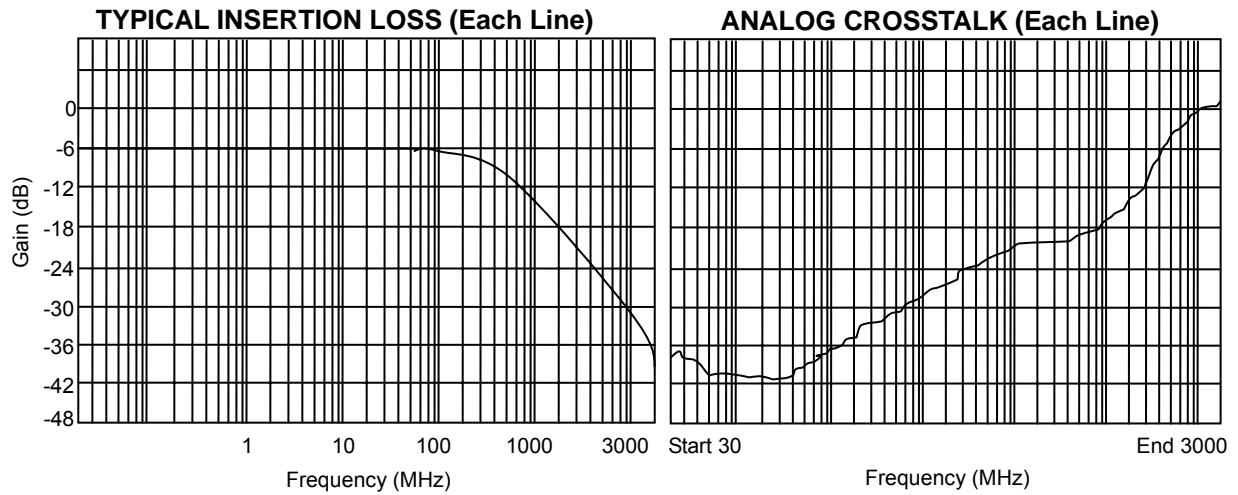
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Stand-off Voltage	Vwm				5.0	V
Breakdown Voltage	Vbr	It=1mA	6.0	8.0	9.5	V
Leakage Current	Ir	Vwm=3V, T=25°C			0.1	μA
Clamping Voltage	Vc	Notes 1,2,3 and 4		12.0		V
Cut-off Frequency (50ohms I/O)	fc	R=100Ω, C=10pF		150		MHz
Minimum attenuation	<>	800-3000MHz	25			dB
Junction Capacitance	Cj	Vr=0V, f=1MHz		20		pF
Total Resistance	R	Each Line		100		Ohms

Note1: ESD applied to input and output pins with respect to GND, one at a time. Note2: Clamping voltage is measured at the opposite side of the EMI filter to the ESD pin. Note3: Unused pins are left open. Note4: Parameter is subjected to design and characterization.

**Uni-Directional Protection**

**Bi-Directional Protection**


**DFN-8 Four Lines EMI Filter Array with TVS Diodes**

**Electrical Characteristics Graphs**



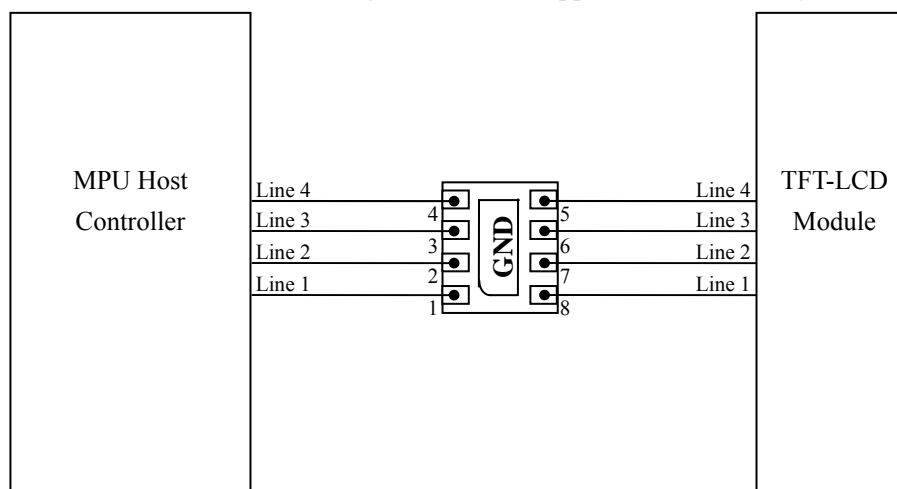
**DFN-8 Hqwt Lines EMI Filter Array with TVS Diodes**

**Applications Information**

UMD4D-100L is comprised of four identical circuits each consisting of a low pass filter for EMI/RFI suppression and dual TVS diodes for ESD protection. This device is in a DFN-8 package. Electrical connection is made to the 8 pins located at the bottom of the device. A center tab serves as the ground connection. The device has a flow through design for easy layout.

Majority of color LCD displays are made with Thin Film Transistors (TFT) and as such are very vulnerable to ESD damage. If an ESD stress hits the TFT display, it will produce a black pixel/line. ESD events can also create Electromagnetic Interference (EMI). EMI radiated from an ESD event can couple into a display through cables or I/O ports and become a voltage or current spike. This spike can then corrupt the operation of the sensitive TFT and affect the display operation and quality. Protection is particularly needed for “flip” phones where data lines are susceptible to ESD at the folding joint.

However the UMD4D-100L is not limited to ESD and EMI filtering at data displays, but can be used anywhere space is limited with a number of data lines that that need to be protected. The UMD4D-100L’s size and form factor makes it a good choice for applications with a large number of data lines.



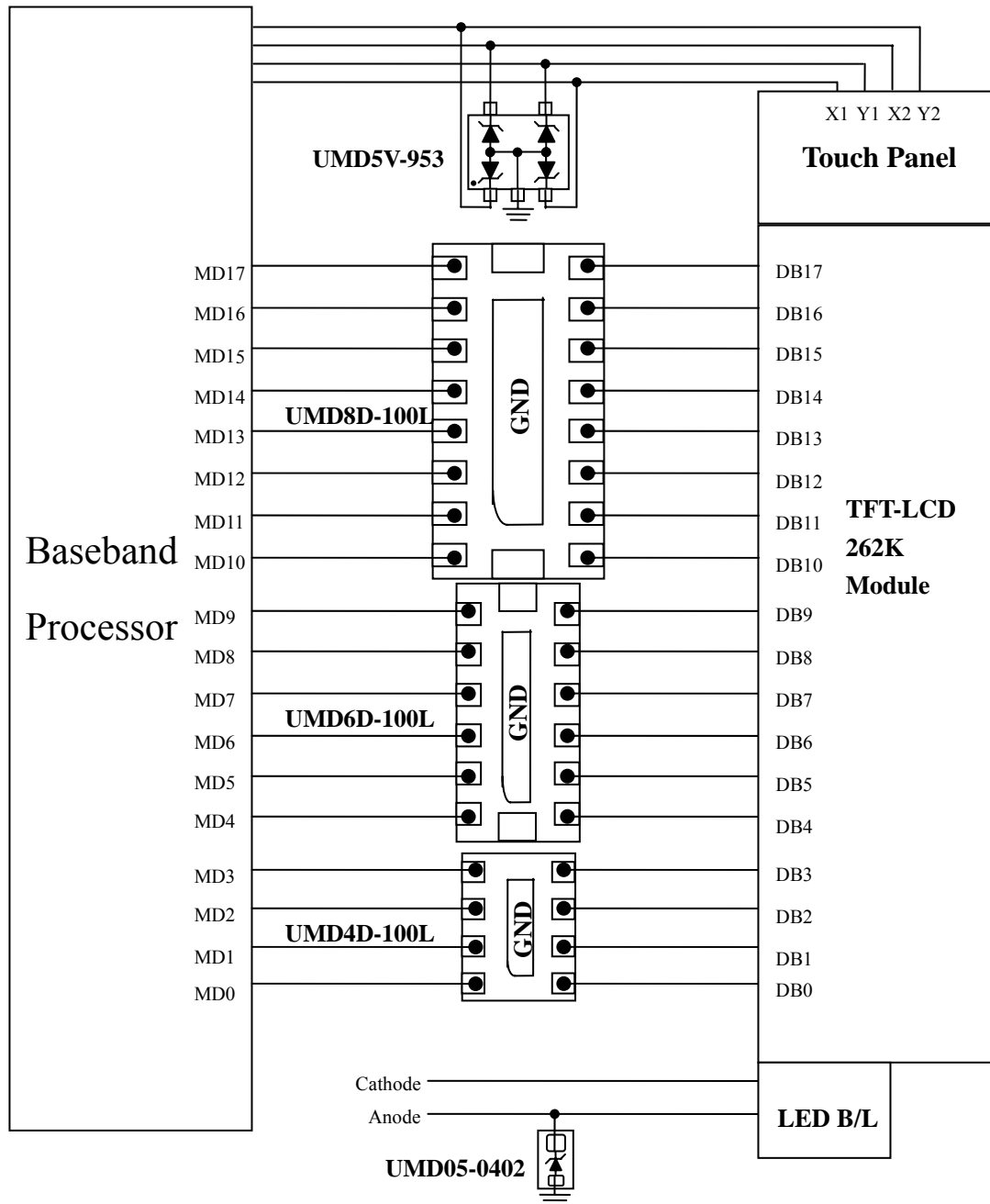
Flow through layout protection

Circuit connectivity is as follows:

- Line 1 is connected to Pin 1 and 8
- Line 2 is connected to Pin 2 and 7
- Line 3 is connected to Pin 3 and 6
- Line 4 is connected to Pin 4 and 5
- Center tab is connected to ground

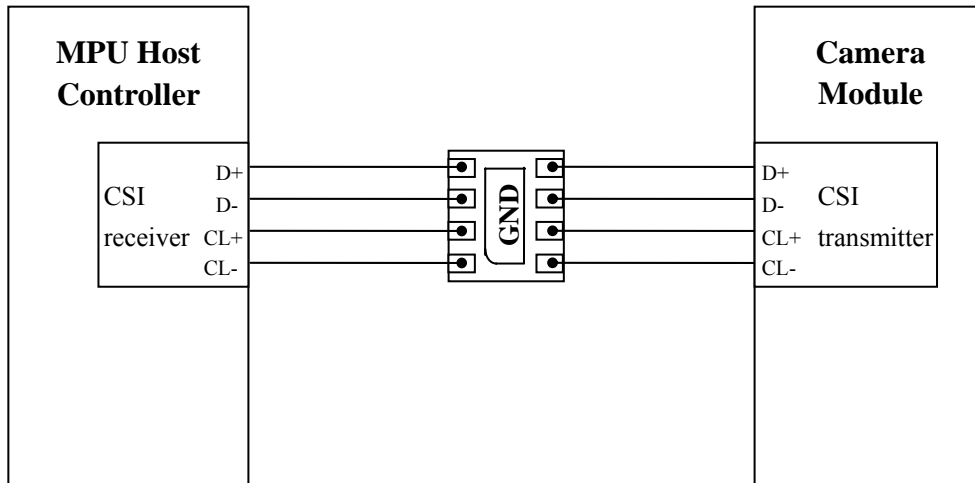
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**UMD4D-100L on TFT-LCD Module Application**

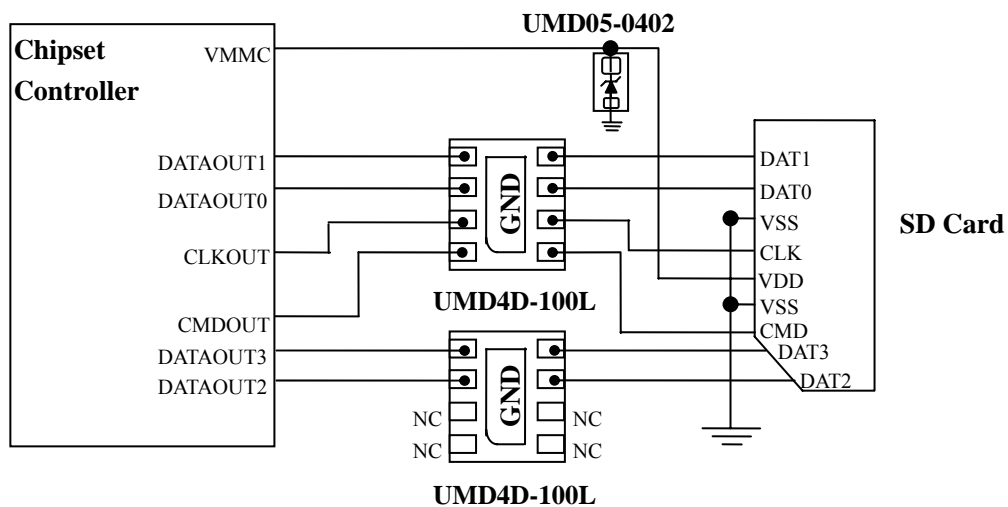
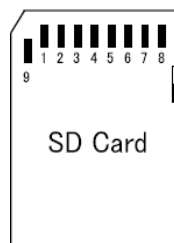


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**UMD4D-100L on Camera Module Protection**



**UMD4D-100L on External Memory Card Protection**



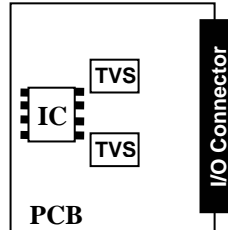
**DFN-8 Hqwt Lines EMI Filter Array with TVS Diodes**

**Circuit Board Layout Recommendations**

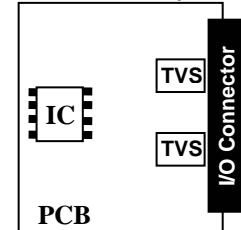
Good circuit board layout is critical for creating an effective surge suppression circuit. The following PCB guidelines are recommended to enhance the performance of a TVS device:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- The ESD transient return path to ground should be kept as short as possible.
- Place a TVS and decoupling capacitor between power and ground of components that may be vulnerable to electrostatic discharges to the ground plane.
- Minimize all conductive loops including power and ground loops.
- Use multilayer boards when possible.
- Minimize interconnecting line lengths.
- Never run critical signals near board edges.
- Fill unused portions of the PCB with ground plane.

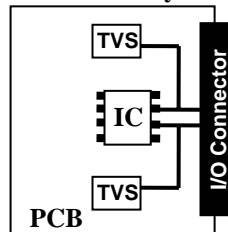
**Poor PCB Layout**



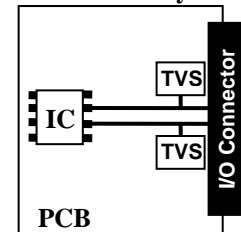
**Good PCB Layout**



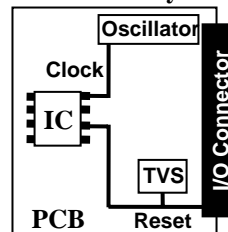
**Poor PCB Layout**



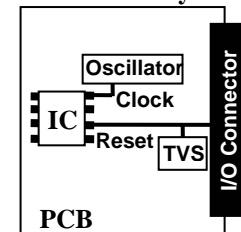
**Good PCB Layout**



**Poor PCB Layout**



**Good PCB Layout**



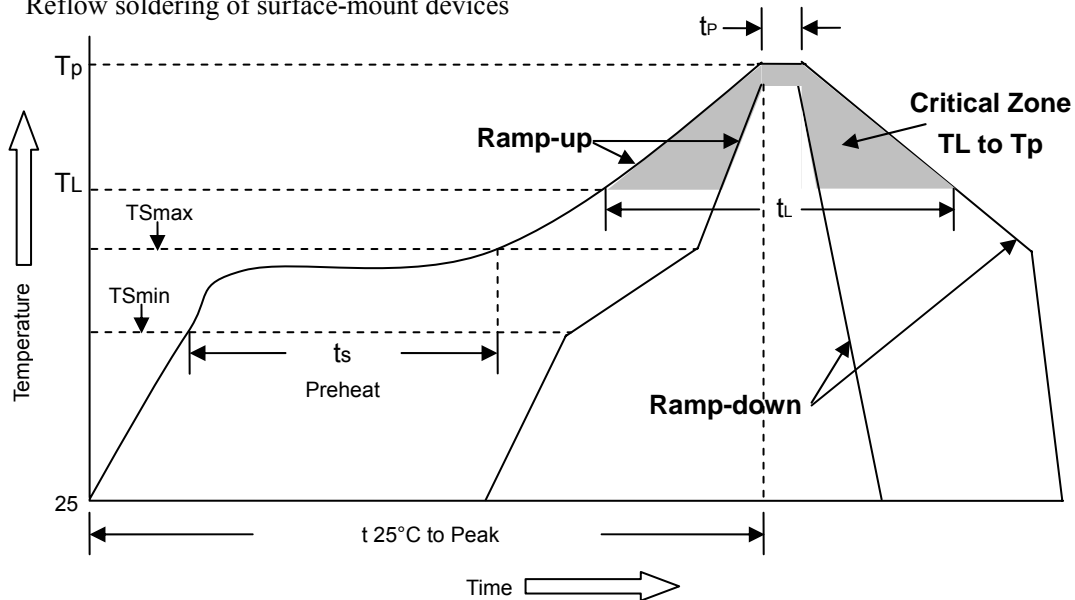
**Matte Tin Lead Finish**

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. Unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation to solder joint.

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**Soldering Method for UMD's Products**

1. Storage environment: Temperature = 10°C~35°C Humidity = 65%±15%
2. Reflow soldering of surface-mount devices



Profile Feature	Pb-Free Assembly
Average ramp-up rate (TL to TP)	<3°C/sec
Preheat	
- Temperature Min (TSmin)	150°C
- Temperature Max (TSmax)	200°C
- Time (min to max) (ts)	60~180sec
TSmax to TL	
- Ramp-up Rate	<3°C/sec
Time maintained above:	
- Temperature (TL)	220°C
- Time (tl)	50~145sec
Peak Temperature (Tp)	260°C +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	20~40sec
Ramp-down Rate	<6°C/sec
Time 25°C to peak Temperature	<8 minutes

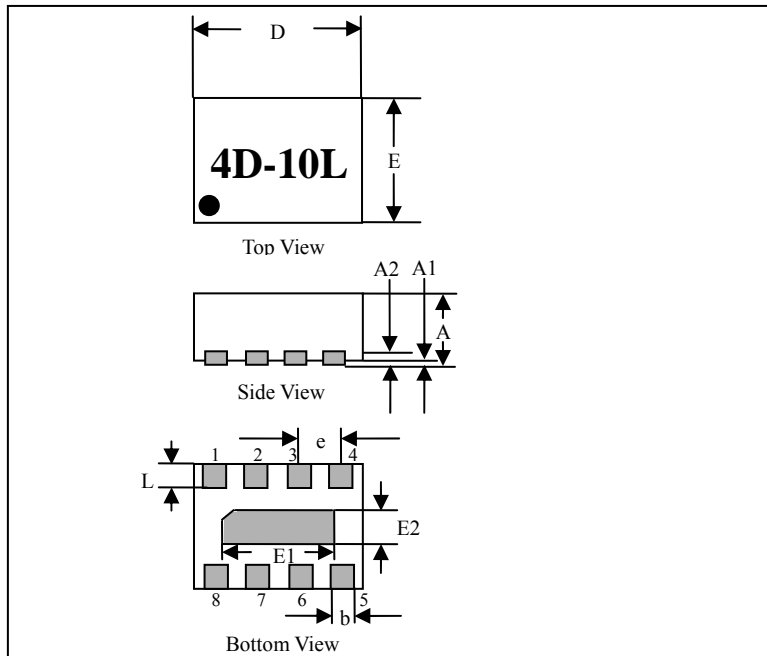
Flow (wave) soldering (solder dipping)

Products	Dipping time
Pb devices	5sec±1sec
Pb-Free devices	5sec±1sec



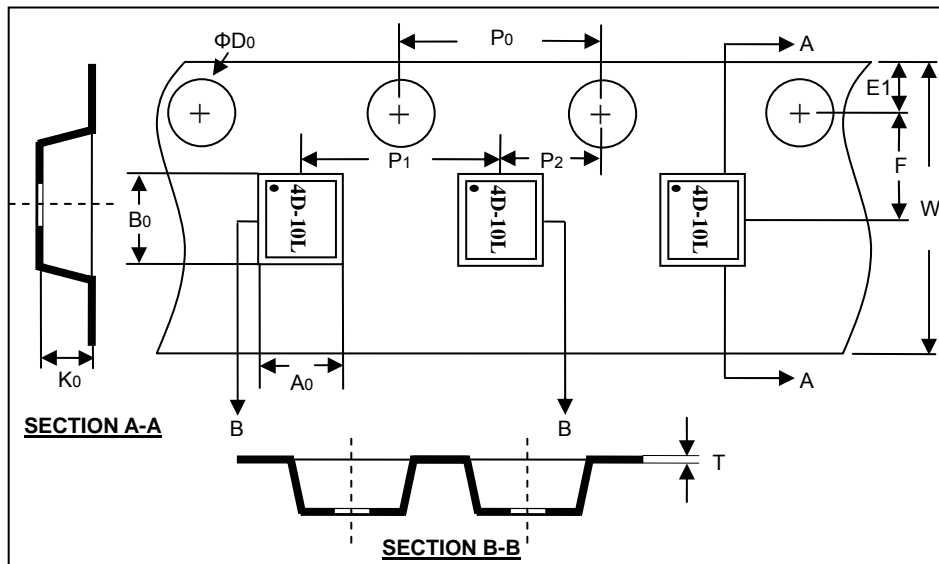
### DFN-8 Hqwt Lines EMI Filter Array with TVS Diodes

### DFN-8 Dimension Drawing

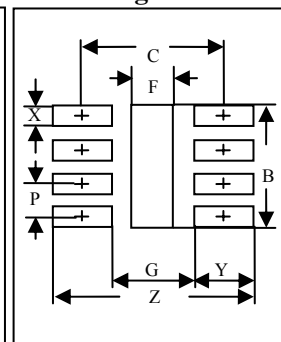


Dim	Dimensions			
	Inches		mm	
	Min	Max	Min	Max
A	0.031	0.035	0.80	0.90
A1	0.000	0.002	0.00	0.05
A2	0.007	0.009	0.18	0.23
L	0.012	0.016	0.30	0.40
D	0.077	0.081	1.95	2.05
E	0.077	0.081	1.95	2.05
e	0.018	0.020	0.46	0.50
b	0.008	0.012	0.20	0.30
E1	0.047	0.048	1.20	1.21
E2	0.022	0.026	0.55	0.65

### DFN-8 Carrier Dimension



### Mounting Pattern



Dim	Typical	
	MM	Inches
Z	2.15	0.085
C	1.52	0.060
G	0.89	0.035
Y	0.63	0.025
X	0.30	0.012
B	1.80	0.071
P	0.50	0.020
F	0.45	0.018

Dimensions in mm.

Reel Dia.	Tape Width	A0	B0	K0	ΦD0	E1
178mm (7")	8mm	2.15±0.10	2.15±0.10	1.00±0.10	1.50±0.10	1.75±0.10
F	W	P0	P1	P2	T	
3.50±0.05	8.00±0.30	4.00±0.10	4.00±0.10	2.00±0.05	0.20±0.05	



**DFN-8 Hqwt Lines EMI Filter Array with TVS Diodes**

**Marking Code**

Part Number	Device Marking
UMD4D-100L	4D-10L

**Ordering Information**

Part Number	Lead Finish	Qty Per Reel	Reel Size
UMD4D-100L	Pb-Free	3,000	7 inch

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