



SOT-523 Dual Lines TVS Array for ESD Protection

Description

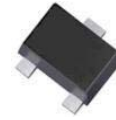
TVS diodes are designed to replace multilayer varistors (MLVs) in portable applications such as cell phones, notebook computers, and PDA's. They offer superior electrical characteristics such as lower clamping voltage and no device degradation when compared to MLVs.

The UMD05T-523 is a TVS array designed to protect I/O or data lines from the damaging effects of ESD. Their integrated design provides very effective and reliable protection for two separate lines using only one package. The SOT-523 is a very small package which allows space saving on high density printed circuit board and also gives the designer the flexibility to provide Uni-Directional or Bi-Directional protection.

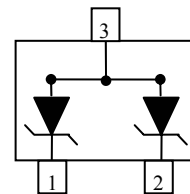
Features

- * Solid-state silicon avalanche technology
- * SOT-523 package
- * Uni-Directional or Bi-Directional protection
- * Protects up to two data lines
- * 150 Watts peak pulse power (tp = 8/20µs)
- * Working voltage: 5V
- * Low clamping factor Vcl/Vbr
- * Low leakage current
- * Full RoHS compliance
- * Complies with the following standards:
 - IEC 61000-4-2 (ESD) Air-15kv, Contact-8kv
 - IEC 61000-4-4 (EFT) (5/50ns)
 - IEC 61000-4-5 (Surge) (8/20µs)

Small Surface Mount Device TVS



SOT-523 Pin Configuration



<u>Pin</u>	<u>Description</u>
1	Cathode
2	Cathode
3	Anode

Mechanical Characteristics

- * Molded SOT-523 package
- * Weight 3 milligrams (Approximate)
- * Available in Lead-Free Pure-Tin Plating
- * Solder Reflow Temp: Pure-Tin (Sn), 260-270°C
- * Consult Factory for Leaded Device Availability
- * Flammability Rating UL 94V-0
- * 8mm Tape and Reel per EIA Standard 481
- * Device Marking: Marking Code,

Applications

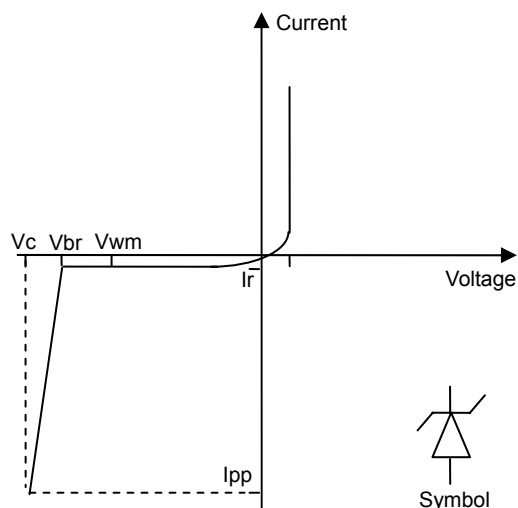
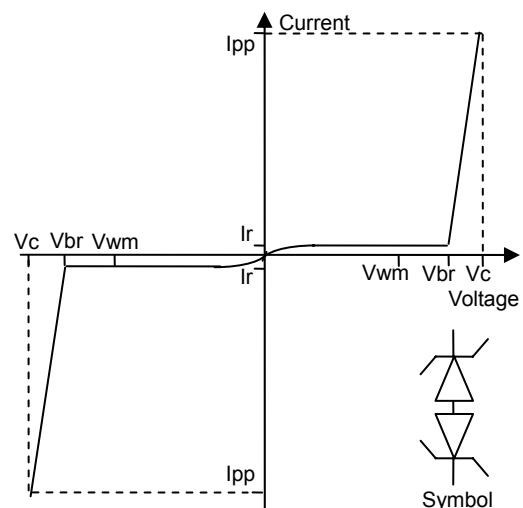
- * Cellular Handset
- * PDA
- * Notebook
- * Digital Camera
- * Wifi Phone
- * Microprocessor Based Equipment

SOT-523 Dual Lines TVS Array for ESD Protection
Absolute Maximum Ratings @ 25°C unless otherwise specified

Parameter	Symbol	Value	Units
Peak Pulse Power; pulse waveform = 8/20µs	Ppp	150	W
Peak Pulse Current; pulse waveform = 8/20µs	Ipp	12	A
ESD per IEC 61000-4-2 (Air)	Vpp	±15	kV
ESD per IEC 61000-4-2 (Contact)		±8	
Operating Temperature	Tj	-55 to 125	°C
Storage Temperature	Tstg	-55 to 150	°C

Electrical Characteristics @ 25°C unless otherwise specified

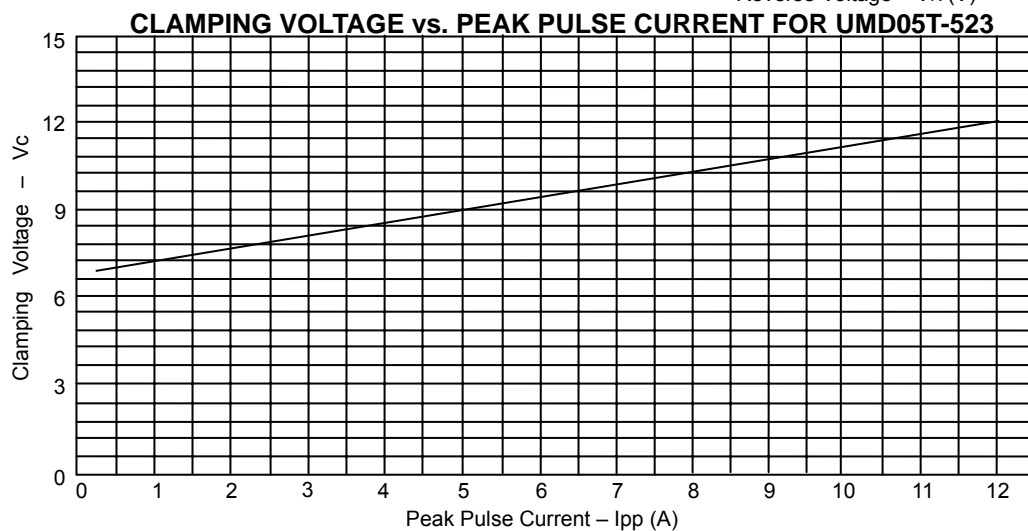
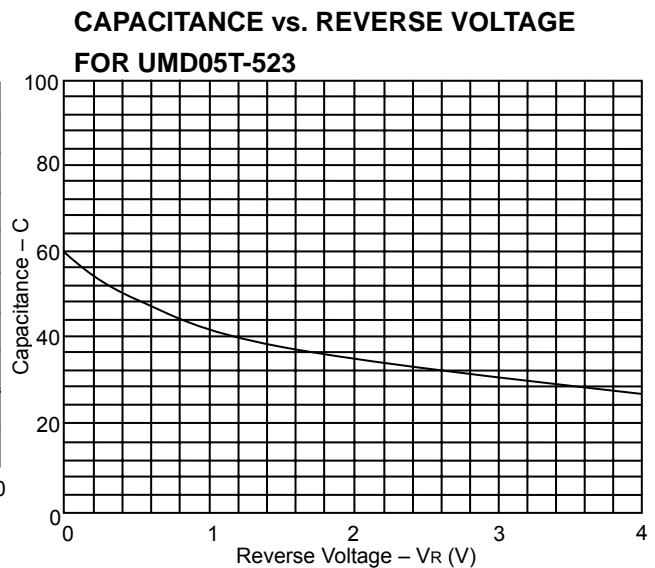
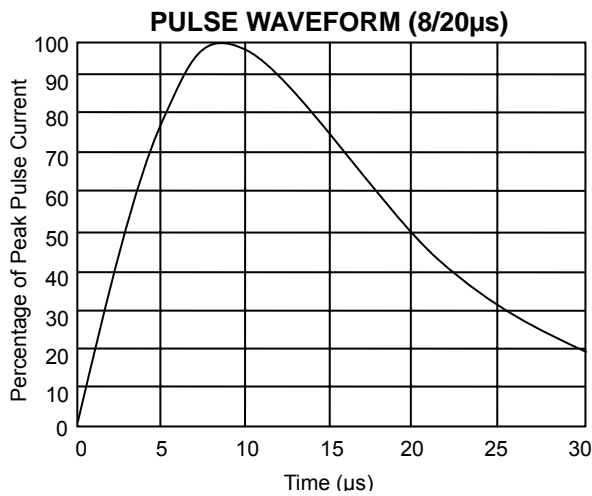
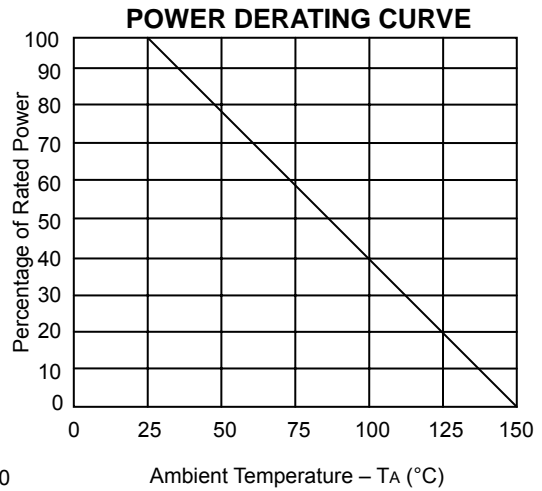
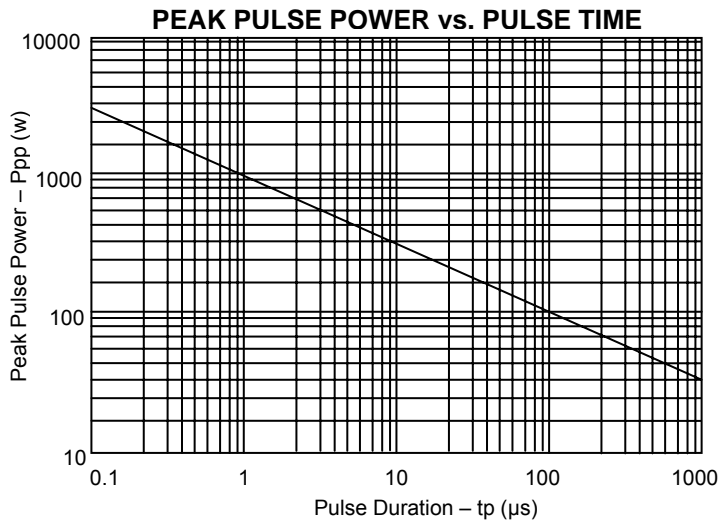
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Stand-off Voltage	Vwm				5.0	V
Breakdown Voltage	Vbr	It=1mA	6.0			V
Leakage Current	Ir	Vwm=5V, T=25°C		0.1	1	µA
Clamping Voltage	Vc	Ipp=1A Tp=8/20µs			7.2	V
Clamping Voltage	Vc	Ipp=12A Tp=8/20µs			12.1	V
Peak Pulse Current	Ipp	Tp=8/20µs			12	A
Junction Capacitance	Cj	Vr=0V, f=1MHz Pin 1 to Pin 2		30		pF
Junction Capacitance	Cj	Vr=0V, f=1MHz Pin 1 or 2 to Pin 3		60		pF

Uni-Directional Protection

Bi-Directional Protection




SOT-523 Dual Lines TVS Array for ESD Protection

Electrical Characteristics Graphs



SOT-523 Dual Lines TVS Array for ESD Protection

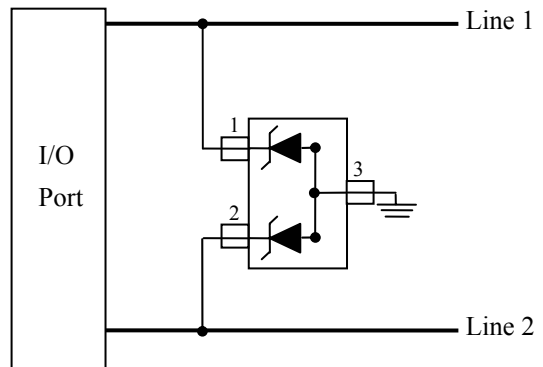
Applications Information

The UMD05T-523 is designed for use in applications where board space is at a premium. Each device requires less than 3.0mm² of PCB area and will protect up to two Uni-Directional lines.

The UMD05T-523 provides up to 2 lines of protection in a common-mode Uni-Directional configuration.

Circuit connectivity is as follows:

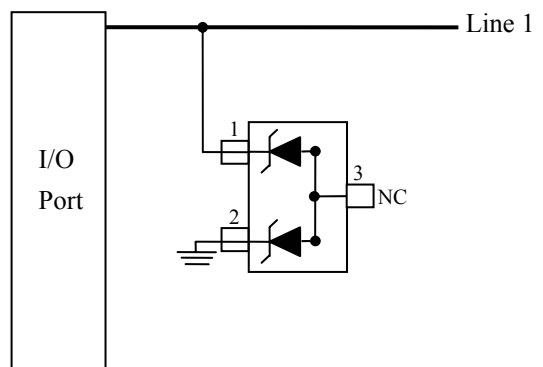
- Line 1 is connected to Pin 1
- Line 2 is connected to Pin 2
- Pin 3 is connected to ground



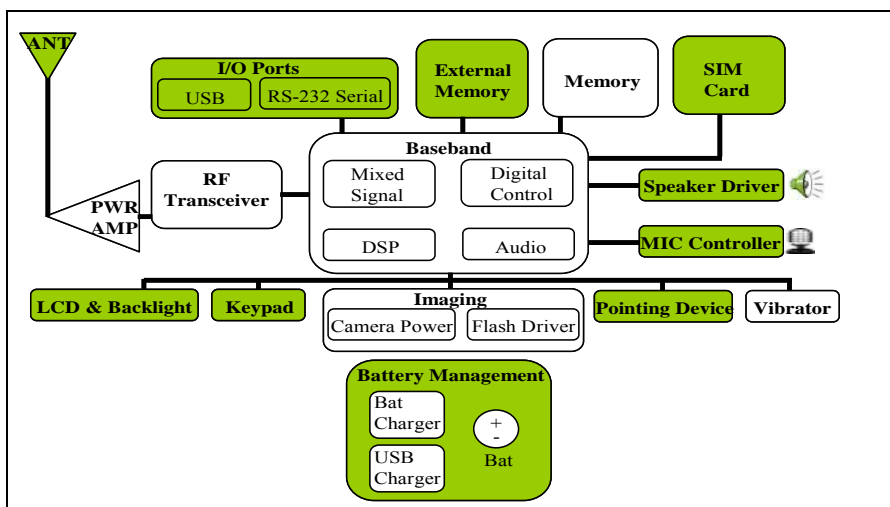
The UMD05T-523 provides single line protection in a common-mode Bi-Directional configuration.

Circuit connectivity is as follows:

- Line 1 is connected to Pin 1
- Pin 2 is connected to ground
- Pin 3 is not connected



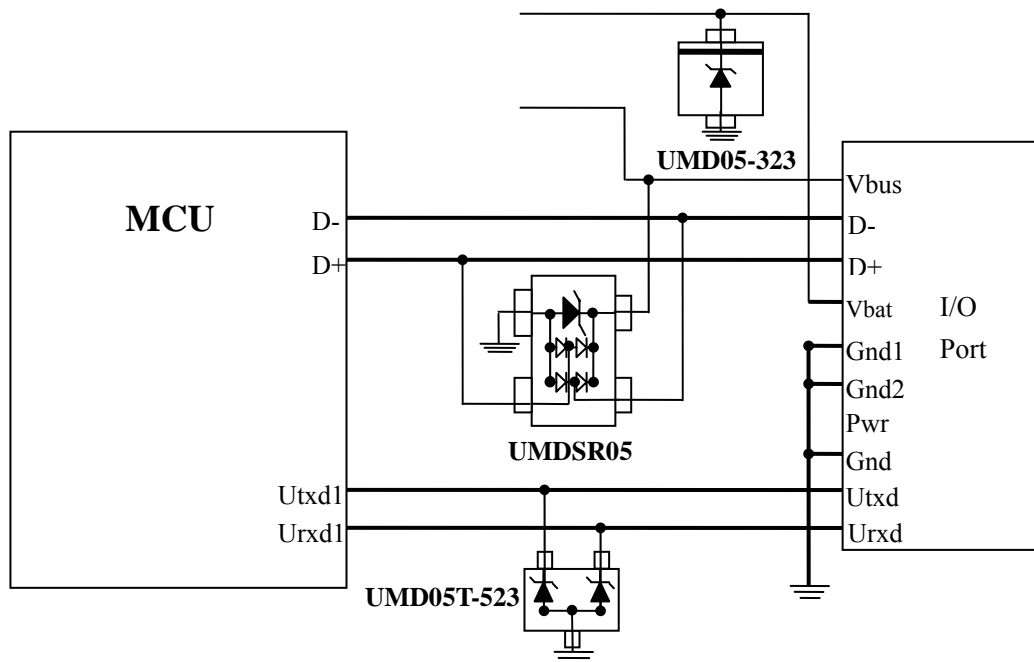
Mobile Handset Block Diagram



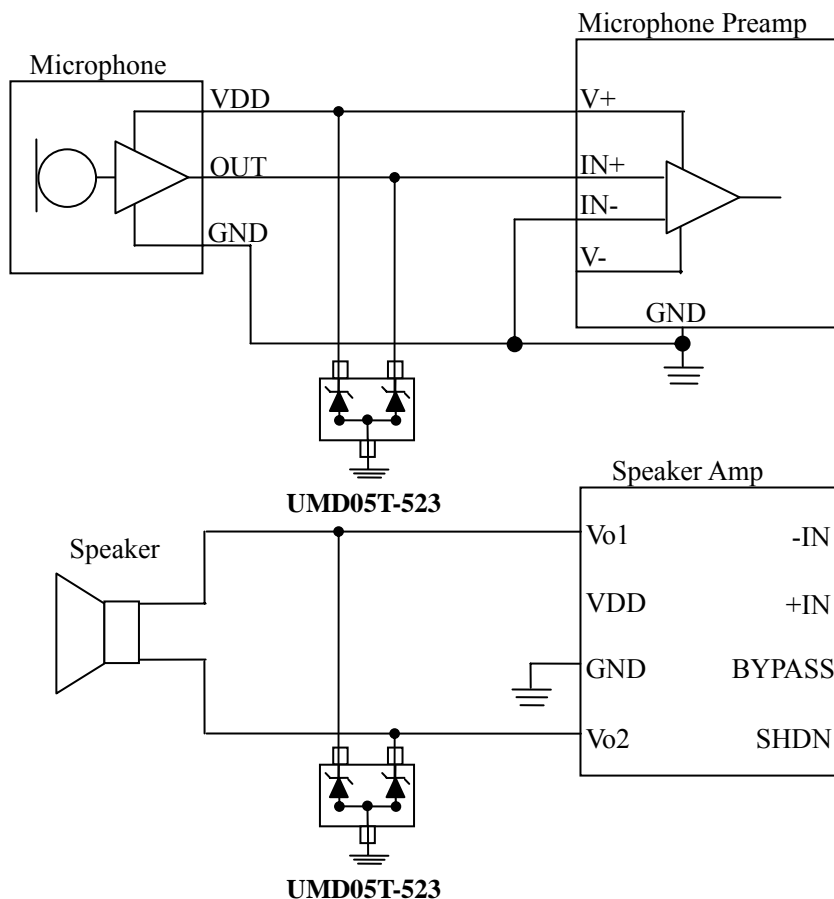
Areas that require ESD protection are highlighted.

SOT-523 Dual Lines TVS Array for ESD Protection

UMD05T-523 on I/O Port Application

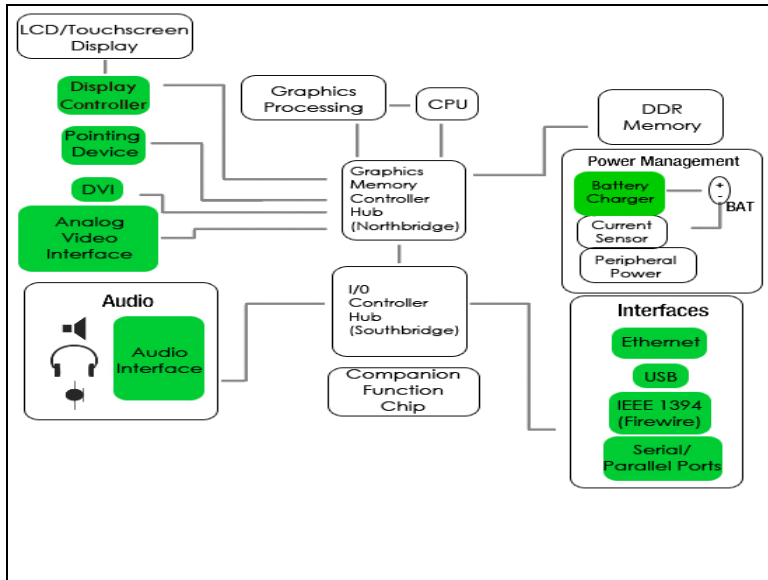


UMD05T-523 on Speaker and Microphone Application



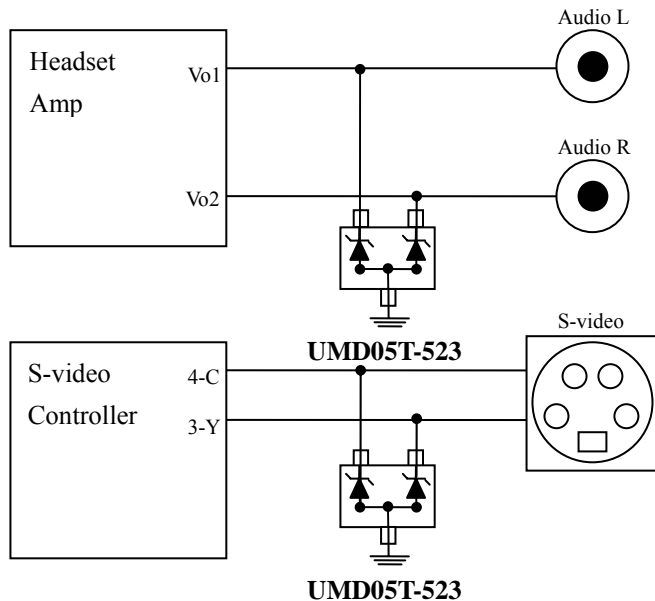
SOT-523 Dual Lines TVS Array for ESD Protection

Laptop Block Diagram



Areas that require ESD protection are highlighted.

UMD05T-523 on S-video and Audio Ports Application



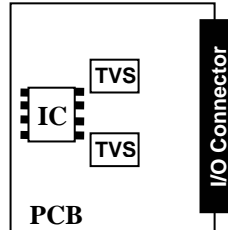
SOT-523 Dual Lines TVS Array for ESD Protection

Circuit Board Layout Recommendations

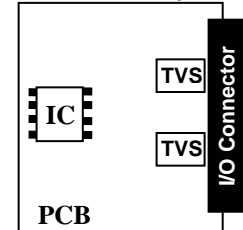
Good circuit board layout is critical for creating an effective surge suppression circuit. The following PCB guidelines are recommended to enhance the performance of a TVS device:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- The ESD transient return path to ground should be kept as short as possible.
- Place a TVS and decoupling capacitor between power and ground of components that may be vulnerable to electrostatic discharges to the ground plane.
- Minimize all conductive loops including power and ground loops.
- Use multilayer boards when possible.
- Minimize interconnecting line lengths.
- Never run critical signals near board edges.
- Fill unused portions of the PCB with ground plane.

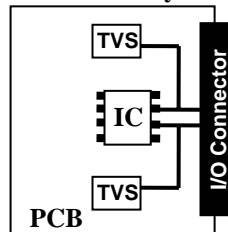
Poor PCB Layout



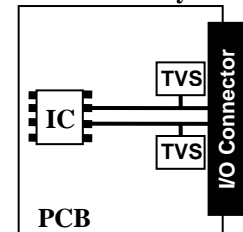
Good PCB Layout



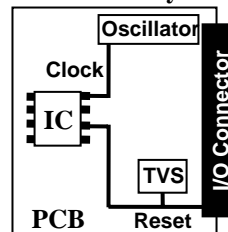
Poor PCB Layout



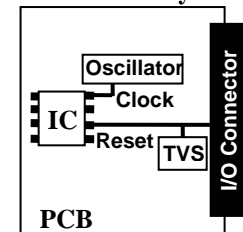
Good PCB Layout



Poor PCB Layout



Good PCB Layout



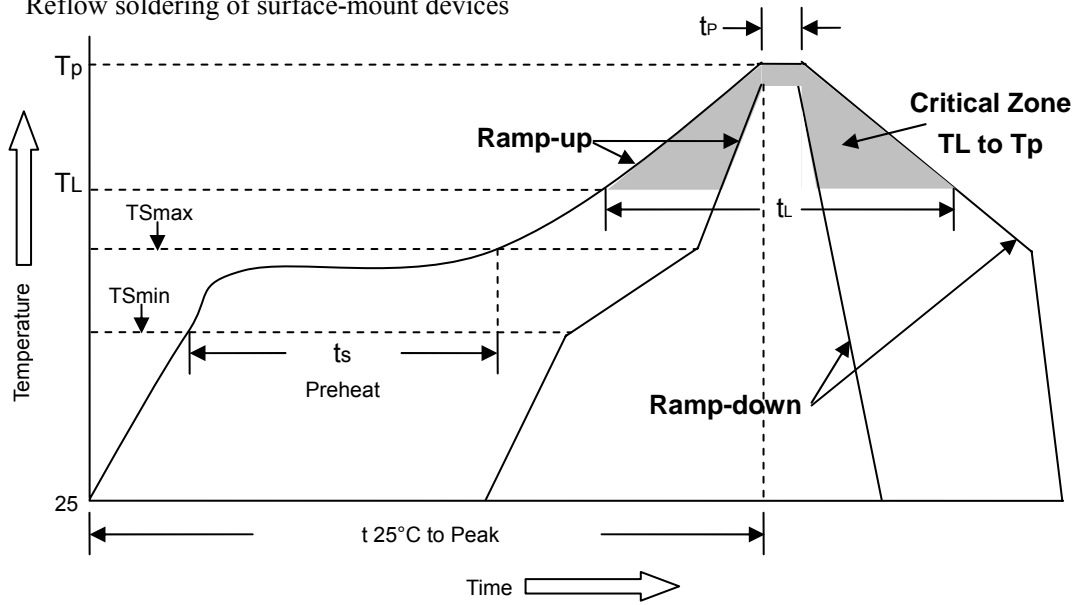
Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. Unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation to solder joint.

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Soldering Method for UMD's Products

1. Storage environment: Temperature = 10°C~35°C Humidity = 65%±15%
2. Reflow soldering of surface-mount devices



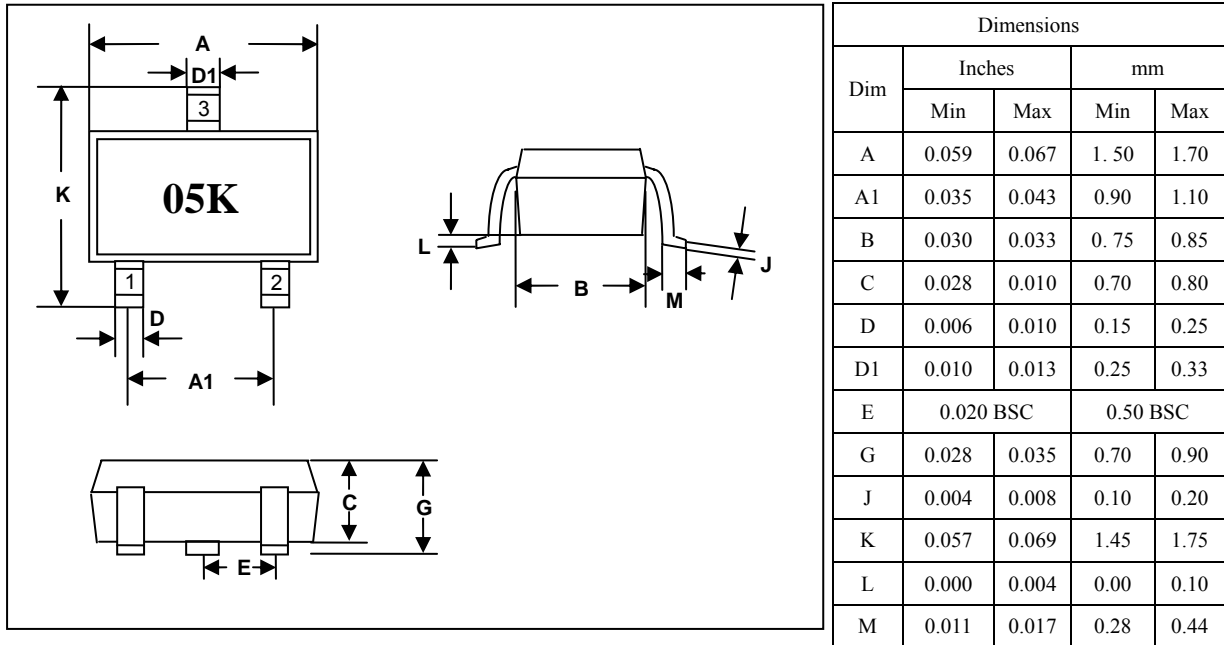
Profile Feature	Pb-Free Assembly
Average ramp-up rate (TL to TP)	<3°C/sec
Preheat	
- Temperature Min (T _{Smin})	150°C
- Temperature Max (T _{Smax})	200°C
- Time (min to max) (t _s)	60~180sec
T _{Smax} to TL	
- Ramp-up Rate	<3°C/sec
Time maintained above:	
- Temperature (TL)	220°C
- Time (t _L)	50~145sec
Peak Temperature (T _P)	260°C +0/-5°C
Time within 5°C of actual Peak Temperature (t _P)	20~40sec
Ramp-down Rate	<6°C/sec
Time 25°C to peak Temperature	<8 minutes

Flow (wave) soldering (solder dipping)

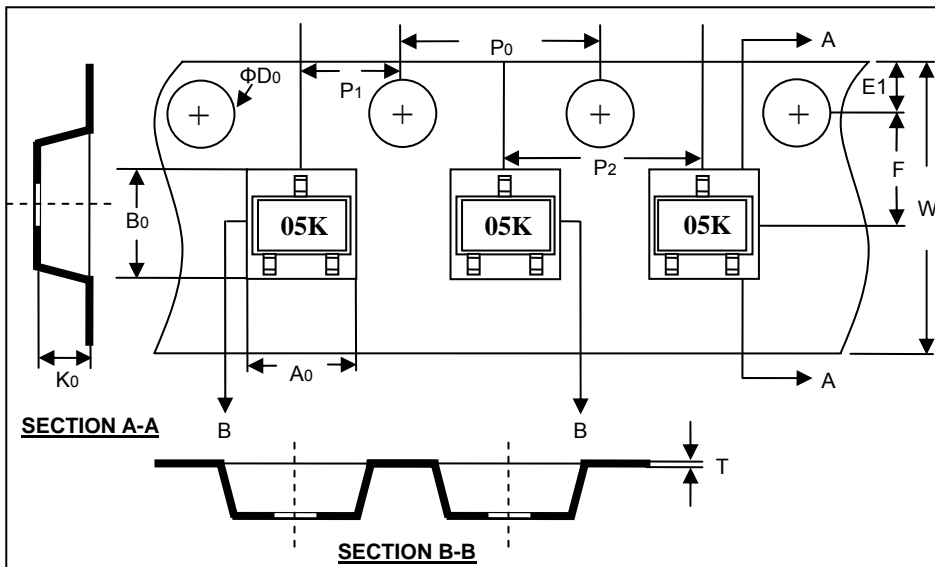
Products	Dipping time
Pb devices	5sec±1sec
Pb-Free devices	5sec±1sec

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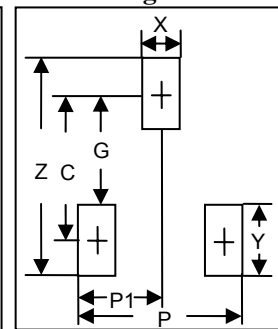
SOT-523 Dimension Drawing



SOT-523 Carrier Dimension



Mounting Pattern



Typical		
Dim	MM	Inches
C	1.40	0.055
P	1.00	0.039
P1	0.50	0.020
G	0.60	0.024
X	0.40	0.016
Y	0.80	0.031
Z	2.20	0.087

Dimensions in mm.

Reel Dia.	Tape Width	A0	B0	K0	ΦD0	E1
178mm (7")	8mm	1.85±0.05	1.85±0.05	0.95±0.05	1.50±0.10	1.75±0.10
F	W	P0	P1	P2	T	
3.50±0.05	8.00±0.30	4.00±0.10	2.00±0.05	4.00±0.10	0.23±0.02	



SOT-523 Dual Lines TVS Array for ESD Protection

Marking Code

Part Number	Device Marking
UMD05T-523	05K

Ordering Information

Part Number	Lead Finish	Qty Per Reel	Reel Size
UMD05T-523	Pb-Free	3,000	7 inch

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